

ABSTRACT OF THE INVENTION

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The present invention includes an automatic scan test enable signal assertion system and method. An automatic scan test enable signal assertion system and method of the present invention responds to transitions in signals communicated via selected pins that are not dedicated solely to testing operations. During testing operations a first selected pin is utilized to communicate a trigger signal (e.g., a PCI reset signal) and a second selected pin is utilized to communicate a stage progression signal (e.g., a PCI clock signal). The trigger signal provides an indication to initiate a scan test enable signal assertion or deassertion and the stage progression signal controls the progress of the scan test enable activation or deactivation initiation. A scan test enable trigger sensing component provides an assertion or deassertion notification when logical values of a trigger signal captured during multiple stages provide an indication to begin a scan test enable signal assertion or deassertion. A staging component advances the logical values through stages in accordance with a progression signal and issues an asserted or deasserted scan test enable signal based upon said assertion or deassertion notification from the scan test enable trigger sensing component.